REMARKS

Reconsideration of the above referenced application in view of the following remarks is requested. In the Specification, paragraphs [0017-18] and [0029] have been amended. Claim 26 has been amended. Existing claims 8-38 remain in the application. Please note that the prosecuting attorney for this application has been changed.

ARGUMENT

Drawings

The drawings are objected to under 37 CFR 1.83(a) because they fail to depict the necessary structural implementation and/or protocol detail essential for the proper understanding of the disclosed invention; see MPEP § 608.02(d).

More specifically, the Examiner asserted that the drawings "lack sufficient detail necessary to enable the understanding of how the claimed invention functionally and correspondingly structurally differs from otherwise well understood local or global cache implementations maintaining ownership tags based upon global read/request-for-ownership (RFO) requests and/or corresponding grants typically utilized to maintain local cache coherence within multi-processor distributed cache implementations ...." The Examiner requests that a sufficiently detailed depiction of a processor comprising the structural means and coupling of a first and second storage unit and bus agent must be shown or the features be cancelled from the claims. Applicants respectfully disagree.

FIG. 2 in the present application shows a cache memory 217 and an embodiment of the subject matter disclosed in the present application 206 along with a

processor 205. FIGs. 4 and 5 further show details of an embodiment of the disclosed subject matter including a global observation store buffer (GoSB) (e.g., 401), a non-committed store queue (NcSQ) (e.g., 415), a line-fill buffer (LFB) (e.g.,) 420 a the level-1 (L1) cache (e.g., 425), and a store buffer (e.g., 430) and their relationships. These figures together provide sufficient details to enable a person of ordinary skill in the art to implement the subject matter disclosed in the present application. Applicants hope that the Examiner did not request Applicants to provide physical implementation details of a buffer as a person of ordinary skill in the art would have known who to implement a buffer in a processor or a computer system. Thus, Applicants respectfully request that the objection to the drawings be withdrawn.

Specification

Paragraph [0029] is objected to as it is considered well understood by those of ordinary skill in the art that a key differentiation between a "processor" and generic logic is not whether it performs an operation as a result of receiving signals or instructions, but whether or not it itself further controls their generation. Corrective action is required.

Paragraph [0029] has been amended. As a result, this rejection is now moot.

Claim Rejections – 35 U.S.C. § 112

Claims 8-38 are rejected per 35 U.S.C. § 112, first paragraph, as based on a disclosure that is not enabling. As elements critical or essential to the practice of the invention are neither included in the claims nor enabled by the disclosure. See In re Mayhew, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Application No.: 10/813,942   Page 12 of 17   Examiner: Schlie, P.
Filed: 03/30/2004   Art Unit: 2186

PAGE 17/22 * RCVD AT 4/20/2007 8:03:03 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/45 * DNIS:2738300 * CSID:5033561415 * DURATION (mm-ss):03-06

Particularly, the Examiner states, "as no method, means, or corresponding structure as presumed to be required to enable subsequent loads which may correspond to the stores which were alternatively chosen to be spilled into a globally visible non-committed store queue and/or corresponding buffer (cache) in lieu of the local cache (also presumably needing to maintain global coherency) may be subsequently globally observed; and no structure or corresponding methods presumably needed to maintain coherency between potentially multiple processor local caches and said globally visible queue/buffer (cache) as presumed to be the context of the claimed invention has been disclosed; thereby lacking critical elements necessary to enable one of ordinary skill in the art to make and/or use the claimed invention without undue experimentation."

Applicants here respectfully disagree. If Applicants understand correctly, the Examiner here requires disclosure of subsequent loads and ways to maintaining cache coherency when the subject matter disclosed in the present application is implemented. It should be noted that data stored in the globally visible non-committed store queue and/or corresponding buffer will eventually be stored in local buffer. The alternative buffer/store queue exists to make the out-of-order RFO possible to use the store latency efficiently. Thus, the subsequent loads and cache coherency is basically the same as before and there is no need for such special disclosures. Accordingly, Applicants request that the 35 U.S.C. § 112 rejections of claims 8-38 be withdrawn.

Claim 26 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such

Application No.: 10/813,942   Page 13 of 17   Examiner: Schlie, P.
Filed: 03/30/2004   Art Unit: 2186

PAGE 18/22 * RCVD AT 4/20/2007 8:03:03 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/45 * DNIS:2738300 * CSID:5033561415 * DURATION (mm-ss):03-06

as omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. As it is not clear what is intended by claiming a computer system wherein the first bus agent comprises an apparatus chosen from a list comprising "a wireless storage medium." Clarification or correction is required.

Claim 26 has been amended. As a result, this rejection is now moot.

Claim Rejections – 35 U.S.C. § 102

Claims 8, 18, 27 and 31 are rejected under 35 U.S.C. § 102(b) as being anticipated by Witek et al. (US 5,043,886) (hereinafter Witek).

The Examiner asserted that figures 1-4 and col. 2, lines 43-68 of Witek disclose, expressly or implicitly, every limitation recited in each of independent claims 8, 18, 27, and 31. Applicants respectfully disagree. In the Examiner's response to Applicants previous arguments used to traverse the same 35 U.S.C. § 102 rejections of these claims, the Examiner states, "As Witek is considered to teach, as effectively acknowledged by the applicant in the traverse of the rejection, a means by which a value and corresponding ownership local to a processor may be made globally visible (to plurality of processors) by utilizing Request/Read-For-Ownership (RFO) semantics; where as Witek does not limit the teaching to strongly or weakly ordered implementations, no such limitation is presumed assuming appropriate safeguards are maintained to warrant coherency; thereby the applicant's claims are considered inherently taught by Witek and merely expressed in other form in absents of any material explanation of some novelty derived capability of utility otherwise (as although the applicant seems to assert a novelty associated with an out-of-order grant of RFO for

a strongly ordered system, in fact such an implementation may be viewed as a weakly ordered system in this respect, thereby the novelty claimed is in fact indistinguishable from an implementation of RFO in weakly ordered system which the applicant is considered to correspondingly indirectly acknowledge as being known as being implicitly identifiable as those which are not strongly ordered RFO implementations)." Applicants must admit here that it is extremely difficult to parse such a single long sentence. To be very honest, Applicants are not sure what the Examiner's main points are here. In case Applicants misunderstand the Examiner, please point such misunderstanding in the next office action.

As Applicants understand, the Examiner basically asserts that Witek implicitly teaches all of the limitations in claims 8, 18, 27, and 31 simply because Witek discloses that a value and corresponding ownership local to a processor may be made globally visible by utilizing RFO semantics. If Applicants' understanding is correct here, Applicants must disagree with the Examiner here. Claim 8 states, "A processor having a strong ordering instruction architecture comprising: a store buffer from which a second data value is to be read and stored to a cache memory *regardless of whether a first data value that is to be read from the store buffer prior to the second data value being read from the store buffer has been globally observed*" (emphases added). What is claimed here is not using RFO to make something globally visible. In fact, nothing in the claim language expressly or implicitly says that. What is claimed here are some out-of-order operations in a processor with ordered store operations. Specifically (as disclosed in the specification), the RFO part of the store operations are made out-of-order according to an embodiment of the subject matter disclosed in the present

Application No.: 10/813,942   **Page 15 of 17**   Examiner: Schlie, P.
Filed: 03/30/2004   Art Unit: 2186

application. The independent claims recite the out-of-order features introduced to the

ordered store operations by the subject matter disclosed in the present application.

Applicants see nothing in Witek, especially the cited portion of Witek, teaches expressly

or implicitly such limitations which combine out-of-order features with store operations.

The Examiner's arguments regarding the weakly ordered system do not seem relevant

here because the out-of-order features here are in the store operations, which in the

end is still in order. The Examiner's arguments are not supported by Witek either since

it does not teach strongly or weakly ordered system, especially based on the cited

portion of Witek.

Because Witek does not teach, expressly or implicitly, every limitation recited in

independent claims 8, 18, 27, and 31, these claims are thus not anticipated by Witek.

Thus, Applicants here respectfully request that the 35 U.S.C. § 102 rejections of claims

8, 18, 27, and 31 be withdrawn.

Claim Rejections – 35 U.S.C. § 103

Claims 9-17, 19-25, 28-30, and 32-38 are rejected under 35 U.S.C. § 103(a) as

being unpatentable over Witek.

Because Witek does not teach, expressly or implicitly, every limitation recited in

independent claims 8, 18, 27, and 31 based on reasons presented above in traversing

the 35 U.S.C. § 102 rejections of these claims, and because there is no other

references cited or common knowledge asserted to cure those deficiencies in Witek,

Witek does not make all of the claims that depend therefrom obvious under 35 U.S.C. §

103(a). Therefore, claims 9-17, 19-25, 28-30, and 32-38, being dependent from claims

Application No.: 10/813,942   **Page 16 of 17**   Examiner: Schlie, P.
Filed: 03/30/2004   Art Unit: 2186

8, 18, 27, and 31, respectively, are patentable over Witek. Accordingly, Applicants

respectfully request that the 35 U.S.C. § 103 rejections of claims 9-17, 19-25, 28-30,

and 32-38 over Witek be withdrawn.

CONCLUSION

Based on the foregoing, it is submitted that that all active claims are presently in

condition for allowance, and their passage to issuance is respectfully solicited. If the

Examiner has any questions, the Examiner is invited to contact the undersigned at (503)

264-1700. Entry of this amendment is respectfully requested.

Respectfully submitted,

Date: ___April 20, 2007___   /Guoujun Zhou/____
                                  Guojun Zhou
                                  Registration No. 56,478
                                  INTEL CORPORATION
                                  MS JF3-147
                                  2111 NE 25th Ave.
                                  Hillsboro, OR. 97124

Application No.: 10/813,942   Page 17 of 17   Examiner: Schlie, P.
Filed: 03/30/2004   Art Unit: 2186